

Optical Interconnection Design Innovator

800GbE to 4x200GbE (OSFP to OSFP RHS) breakout Direct Attach Cable P/N: GOS-4OP801-XXC

Features

- ✓ Hot-plug OSFP CTHS and OSFP RHS form factor
- ✓ Support 8x 50/100Gb/s PAM4 modulation
- ✓ Commercial case temperature range of 0°C to 70°C
- ✓ 26 AWG ~30 AWG support up to 2m length above
- ✓ Contain EEPROM & programmable to customized

Applications

- ✓ Data storage and communication industry
- ✓ Switch / Router / HBA/NIC
- ✓ Enterprise network
- ✓ Data Center Network
- Infiniband

STANDARDS COMPLIANCE

- ✓ IEEE P802.3ck D3.0
- ✓ OSFP MSA HW Rev 4.1
- ✓ ROHS

Description

Gigalight's GOS-4OP801-xxC cable assembly splitter is effective alternative to fiber optics. The cable connects data signals from each of the 16 pairs on the single OSFP end to the quad OSFP RHS ends, each pair operates at data rates of up to 100Gb/s, each OSFP/OSFP RHS port can be addressed by EEPROM to provide product information, which can be read or write by I2C interface.

Gigalight's GOS-4OP801-xxC cable assembly splitter is compliant with the OSFP-MSA and IEEE 802.3ck, it's a high performance, lowest-cost &latency &power consumption I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet and exceed 800 Gigabit Ethernet, InfiniBand EDR /HDR/NDR and temperature requirements for performance and reliability.

The height of OSFP CTHS (Close Top Heat Sink) is fully compliant with OSFP finned top, OSFP RHS(Riding Heat Sink) also can be called flat top, it's a little bit lower than OSFP CTHS.



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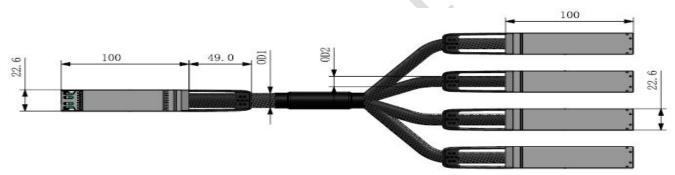
Absolute Maximum Ratings

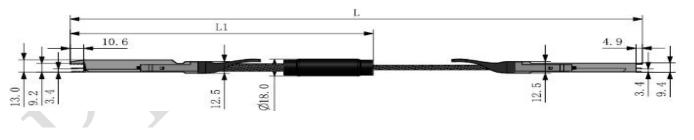
Parameter	Symbol	Min	Мах	Unit
Storage Temperature	Ts	-20	85	°C
Case Operating Temperature	Tc	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

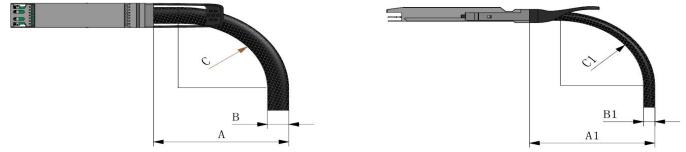
Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Мах	Unit
Operating Case Temperature	Tc	0	6	70	°C
Baud Rate per Lane (PAM4)	fd		53.125		GBaud/s
Humidity	Rh	5		85	%

Mechanical Dimensions







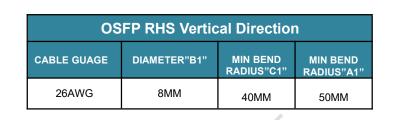


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OSFP Horizontal Direction				
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"	
26AWG	11MM	55MM	65MM	

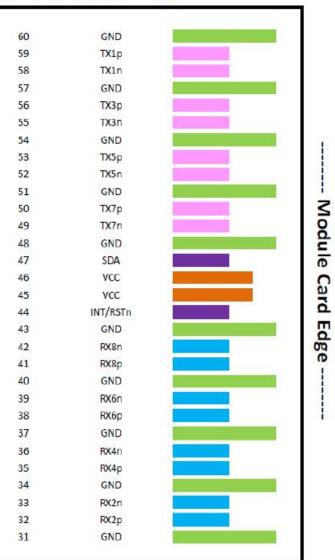
OSFP Electrical pinout

Top Side (viewed from top)



Bottom Side (viewed from bottom)

GND 1 TX2p 2 3 TX2n GND 4 5 TX4p TX4n б 7 GND ТХбр 8 9 TX6n GND 10 TX8p 11 TX8n 12 GND 13 SCL 14 VCC 15 VCC 16 LPWn/PRSn 17 GND 18 RX7n 19 RX7p 20 GND 21 RX5n 22 RX5p 23 GND 24 RX3n 25 **RX3**p 26 GND 27 RX1n 28 RX1p 29 GND 30



Electrical pin list and description



深圳市易飞扬通信技术有限公司 Shenzhen Gigalight Technology Co., Ltd.

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Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
8	GND	Ground Transmitter Data Non-Inverted	CML-I	Input from Host	1	
9	TX6p TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground	CIVIL-I	input ironi Host	1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground	Citic I	inpactionitiosc	1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull- up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground		~	1	
1 22	DVDe	Dessiver Date Man Invested	CNALO	Output to Uport	2	
32 Pin#	RX2p Symbol	Receiver Data Non-Inverted Description	CML-O Logic	Output to Host	3 Plug	Notes
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
Pin# 33	Symbol RX2n	Description Receiver Data Inverted			Plug Sequence 3	Notes
Pin# 33 34	Symbol RX2n GND	Description Receiver Data Inverted Ground	Logic CML-O	Direction Output to Host	Plug Sequence 3 1	Notes
Pin# 33 34 35	Symbol RX2n GND RX4p	Description Receiver Data Inverted Ground Receiver Data Non-Inverted	Logic CML-0 CML-0	Direction Output to Host Output to Host	Plug Sequence 3 1 3	Notes
Pin# 33 34 35 36	Symbol RX2n GND RX4p RX4n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted	Logic CML-O	Direction Output to Host	Plug Sequence 3 1 3 3 3	Notes
Pin# 33 34 35 36 37	Symbol RX2n GND RX4p RX4n GND	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground	Logic CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 3 1	Notes
Pin# 33 34 35 36 37 38	Symbol RX2n GND RX4p RX4n GND RX6p	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted	Logic CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 3 1 3 3 3 3 3 3 3	Notes
Pin# 33 34 35 36 37	Symbol RX2n GND RX4p RX4n GND RX6p RX6n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted	Logic CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 1 3 3 3 3 3	Notes
Pin# 33 34 35 36 37 38 39 40	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 1 3 3 3 1 1	Notes
Pin# 33 34 35 36 37 38 39	Symbol RX2n GND RX4p RX4n GND RX6p RX6n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted	Logic CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 1 3 3 3 3 3	Notes Notes
Pin# 33 34 35 36 37 38 39 40 41	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX6n GND RX8p	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Inverted Ground Receiver Data Non-Inverted	Logic CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3	Notes Notes
Pin# 33 34 35 36 37 38 39 40 41 42	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX6n GND RX8p RX8n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Inverted Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 3 3 3	Notes
Pin# 33 34 35 36 37 38 39 40 41 42 43	Symbol RX2n GND RX4p RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 2 3 1	See pin description
Pin# 33 34 35 36 37 38 39 40 41 42 43 44	Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND INT/RSTn	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Inverted Ground Module Interrupt / Module Reset	Logic CML-O CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3	See pin description for required circuit
Pin# 33 33 34 35 36 37 38 39 40 41 42 43 44 45 45	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Meceiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power	Logic CML-O CML-O CML-O CML-O CML-O CML-O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 2 2	See pin description
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 46	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 2 2 2 2 3 1	See pin description for required circuit
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Direction Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3	See pin description for required circuit
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 50	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-O LVCMOS-I/O	Direction Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2 3 1 3 3 1 3 3 3 3	See pin description for required circuit
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O LVCMOS-I/O	Direction Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2 3 1 3 3 1 1 3 3 1 1 1 3 3 1 1 1 3 3 1	See pin description for required circuit
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 52	Symbol RX2n GND RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX5n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 2 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 3 1 3 3 3 3 3 1 3 3 3 3 3 1 3 3 3 3 3 1 3	See pin description for required circuit
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53	Symbol RX2n GND RX4p RX4p RX4n GND RX6p RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX5n TX5p	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O LVCMOS-I/O	Direction Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 3 3	See pin description for required circuit
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 54	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Hos	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 2 2 2 2 3 1 3 3 1 1 3 3 1 1 1 3 3 1 1 1 3 1	See pin description for required circuit
Pin# 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55	Symbol RX2n GND RX4p RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-I CML-I CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 3 1 3 3 3 3 3 1 3 3 3 3 3 1 3	See pin description for required circuit
Pin# 33 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Hos	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3	See pin description for required circuit
Pin# 33 33 34 35 36 37 38 39 40 41 42 43 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57	Symbol RX2n GND RX4p RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n TX3p GND	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-I CML-I CML-I CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Output from Host	Plug Sequence 3 1 3 3 1 1 3 3 3 1 1 3 3 3 1 1 3 3 3 1 1 3 3 1 1 3 3 3 1 1 3 3 1 1 3 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 11 3 3 1 1 3 1 1 1 3 1	See pin description for required circuit
Pin# 33 33 34 35 36 37 38 39 40 41 42 43 41 44 43 46 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58	Symbol RX2n GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n TX3p GND	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground<	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-I CML-I CML-I CML-I CML-I CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Output from Host	Plug Sequence 3 1 3 3 1 3 3 1 3 3 1 3 3 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 3 1 3 3 3 3 1 3 3 3 3 1 3	See pin description for required circuit
Pin# 33 33 34 35 36 37 38 39 40 41 42 43 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57	Symbol RX2n GND RX4p RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n TX3p GND	Description Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Ground Receiver Data Non-Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground	Logic CML-O CML-O CML-O CML-O CML-O CML-O CML-O CML-I CML-I CML-I CML-I CML-I CML-I	Direction Output to Host Bi-directional Power from Host Bi-directional Input from Host Output from Host	Plug Sequence 3 1 3 3 1 1 3 3 3 1 1 3 3 3 1 1 3 3 3 1 1 3 3 3 1 1 3 3 3 1 1 3 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 3 1 1 1 3 3 1 1 1 3 1	See pin description for required circui



www.gigalight.com Ordering information

Part Number	GQD-PC801-XXXC		
Length (meter)	0.5	1	2
Wire gauge (AWG)	30	30	26

If length(meter) is decimal, PN should be as GOS-4OP801-DXXC, above 2m reach also can be customized.

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice. The publication of information in this data sheet does not imply freedom from patent or other protective rights of Gigalight or others. Further details are available from any Gigalight sales representative.

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Revision History

Revision	Date	Description
V0	Jun-21-2024	Advance Release.