

Optical Interconnection Design Innovator

# 800GbE to 2x400GbE (OSFP to OSFP RHS) Direct Attach Cable P/N: GOS-20P801-XXC

### Features

- ✓ Hot-plug OSFP CTHS and OSFP RHS form factor
- ✓ Support 8x 50/100Gb/s PAM4 modulation
- ✓ Commercial case temperature range of 0°C to 70°C
- ✓ 26 AWG ~30 AWG support up to 2m length above
- ✓ Contain EEPROM & programmable to customized

## Applications

- ✓ Data storage and communication industry
- ✓ Switch / Router / HBA/NIC
- ✓ Enterprise network
- ✓ Data Center Network
- Infiniband

## STANDARDS COMPLIANCE

- ✓ IEEE P802.3ck D3.0
- ✓ OSFP MSA HW Rev 4.1
- ✓ ROHS

## Description

Gigalight's GOS-2OP801-xxC cable assembly splitter is effective alternative to fiber optics. The cable connects data signals from each of the 16 pairs on the single OSFP end to the dual OSFP RHS ends, each pair operates at data rates of up to 100Gb/s, each OSFP/OSFP RHS port can be addressed by EEPROM to provide product information, which can be read or write by I2C interface.

Gigalight's GOS-2OP801-xxC cable assembly splitter is compliant with the OSFP-MSA and IEEE 802.3ck, it's a high performance, lowest-cost &latency &power consumption I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet and exceed 800 Gigabit Ethernet, InfiniBand EDR /HDR/NDR and temperature requirements for performance and reliability.

The height of OSFP CTHS (Close Top Heat Sink) is fully compliant with OSFP finned top, OSFP RHS(Riding Heat Sink) also can be called flat top, it's a little bit lower than OSFP CTHS.



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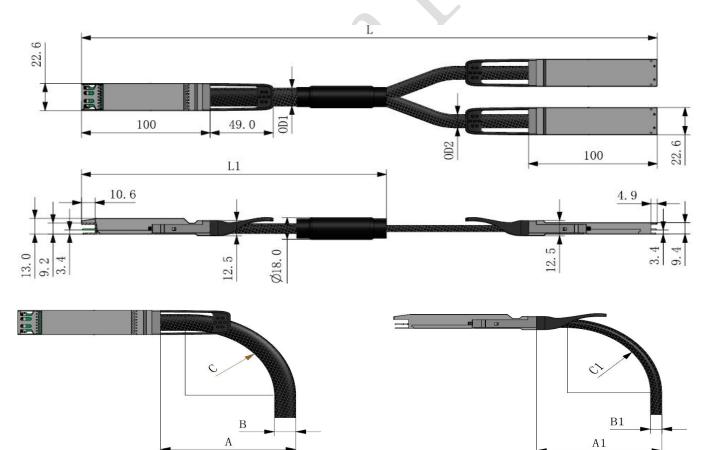
## **Absolute Maximum Ratings**

Parameter	Symbol	Min	Мах	Unit
Storage Temperature	Ts	-20	85	°C
Case Operating Temperature	Tc	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

## **Recommended Operating Conditions**

Parameter	Symbol	Min	Typical	Мах	Unit
Operating Case Temperature	Tc	0	6	70	°C
Baud Rate per Lane (PAM4)	fd		53.125		GBaud/s
Humidity	Rh	5		85	%

## **Mechanical Dimensions**





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CABLE GUAGE

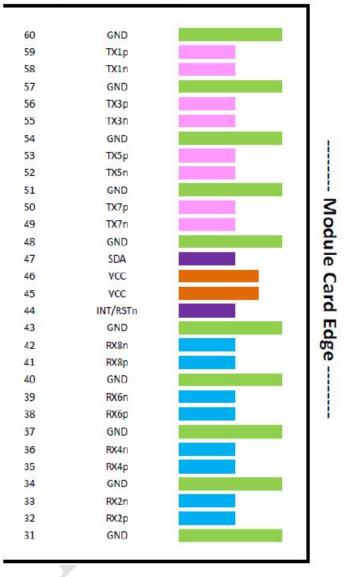
26AWG

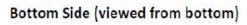
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OSFP Horizontal Direction				
CABLE GUAGE	DIAMETER"B"	MIN BEND RADIUS"C"	MIN BEND RADIUS"A"	
26AWG	11MM	55MM	65MM	

## **OSFP Electrical pinout**

## Top Side (viewed from top)





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MIN BEND

RADIUS"C1

40MM

**MIN BEND** 

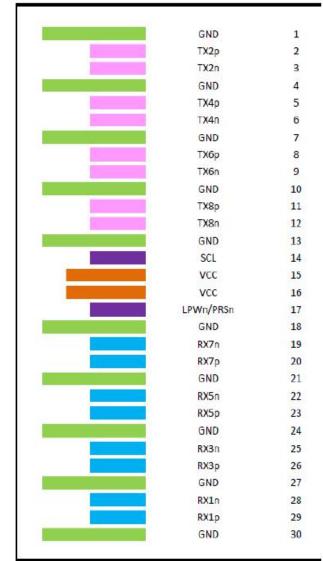
RADIUS"A1"

50MM

**OSFP RHS Vertical Direction** 

DIAMETER"B1"

8MM



## Electrical pin list and description



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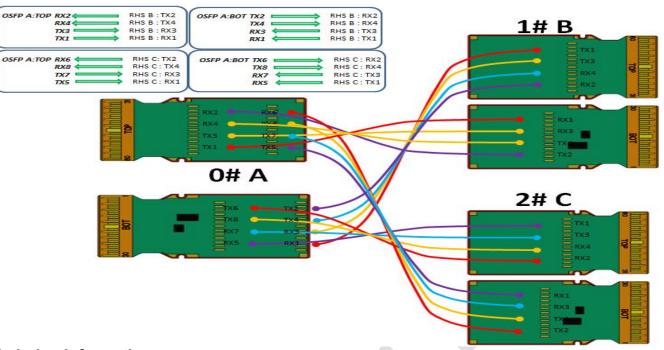
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	ТХ6р	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground	Ch (I) I	In such farmer 11 and	1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground		-	1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull- up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground	Ch II O	O day the line	1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground	Chill O	Outrast to Used	3	
22	RX5n	Receiver Data Inverted Receiver Data Non-Inverted	CML-0 CML-0	Output to Host Output to Host	3	
23	RX5p GND	Ground	CIVIL-0	Output to Host	1	
25	RX3n	Receiver Data Inverted	CML-0	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
27	GND	Ground	CIVIL-O	Output to Host	1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-0	Output to Host	3	
30	GND	Ground	CIVIL-O	output to host	1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground	Citic O	oucput to nost	1	2
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted		ourput to most	-	
37	GND	Receiver Data Inverted	CML-O	Output to Host	3	
38		Ground	CML-0	Output to Host	3	
39	RX6p				8 S	
	RX6p RX6n	Ground	CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host	1	
40		Ground Receiver Data Non-Inverted	CML-0	Output to Host	1 3	
40	RX6n GND	Ground Receiver Data Non-Inverted Receiver Data Inverted	CML-0	Output to Host Output to Host	1 3 3	
	RX6n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground	CML-0 CML-0	Output to Host	1 3 3 1	
41	RX6n GND RX8p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted	CML-O CML-O CML-O	Output to Host Output to Host Output to Host	1 3 3 1 3	
41 42	RX6n GND RX8p RX8n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted	CML-O CML-O CML-O	Output to Host Output to Host Output to Host	1 3 1 3 3 3	See pin description for required circuit
41 42 43 44	RX6n GND RX8p RX8n GND INT/RSTn	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset	CML-0 CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host Output to Host Bi-directional	1 3 1 3 3 1 3	See pin description for required circuit
41 42 43	RX6n GND RX8p RX8n GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground	CML-0 CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host Output to Host	1 3 1 3 3 1	
41 42 43 44 45	RX6n GND RX8p RX8n GND INT/RSTn VCC	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power	CML-0 CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host	1 3 1 3 1 3 1 3 2	for required circuit
41 42 43 44 45 46	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power	CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Power from Host	1 3 1 3 1 3 1 3 2 2 2	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground	CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 1 3 1 3 1 3 2 2 2 3	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data	CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host	1 3 1 3 1 3 2 2 2 3 1	for required circuit Open-Drain with pull-
41 42 43 44 45 46 46 47 48 49	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted	CML-0 CML-0 CML-0 CML-0 Multi-Level LVCMOS-I/0 CML-I	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 1 3 1 3 2 2 2 3 1 3	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 49 50	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted	CML-0 CML-0 CML-0 CML-0 Multi-Level LVCMOS-I/0 CML-I	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host	1 3 1 3 1 3 2 2 2 3 1 3 3 3 3	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 49 50 51 52	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX5n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted	CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host	1 3 3 1 3 1 3 2 2 2 3 1 3 3 1 3 3 1 3	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 49 50 51	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted Ground	CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host	1 3 3 1 3 1 3 2 2 2 3 1 3 3 1 3 1	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 47 48 49 50 51 52 53 54	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX5n TX5p GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground	CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host	1 3 3 1 3 1 3 2 2 2 3 1 3 3 1 3 3 1 3 1	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 47 48 49 50 51 52 53 54 55	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX5n TX5p GND TX5n TX5p GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted	CML-0 CML-0 CML-0 CML-0 Multi-Level LVCMOS-I/0 CML-1 CML-1 CML-1 CML-1 CML-1	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host Input from Host	1 3 3 1 3 1 3 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 47 48 49 50 51 52 53 54 55 56	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX5n TX5p GND TX5n TX5p GND TX3n TX3p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground	CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host	1 3 3 1 3 1 3 2 2 2 3 1 3 3 1 3 3 1 3 1	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 47 48 49 50 51 52 53 54 55 56 57	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX5n TX5p GND TX5n TX5p GND TX3n TX3p GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted	CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Bi-directional Input from Host Input from Host Input from Host Input from Host Input from Host	1 3 3 1 3 1 3 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1	for required circuit Open-Drain with pull-
41 42 43 44 45 46 47 48 47 48 49 50 51 52 53 54 55 56	RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX5n TX5p GND TX5n TX5p GND TX3n TX3p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Ground	CML-0 CML-0 CML-0 CML-0 Multi-Level LVCMOS-I/0 CML-1 CML-1 CML-1 CML-1 CML-1	Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host Input from Host	1 3 3 1 3 1 3 2 2 2 3 1 3 3 1 3 3 1 3 3 1 3 3 3 3	for required circuit Open-Drain with pull-



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#### Wire connection diagram

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### **Ordering information**

Part Number		GQD-PC801-XXXC	
Length (meter)	0.5	1	2
Wire gauge (AWG)	30	30	26

If length(meter) is decimal, PN should be as GOS-2OP801-DXXC, above 2m reach also can be customized.

### **Important Notice**

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice. The publication of information in this data sheet does not imply freedom from patent or other protective rights of Gigalight or others. Further details are available from any Gigalight sales representative.

#### E-mail: sales@gigalight.com

Official Site: <u>www.gigalight.com</u> **Revision History** 

Revision	Date	Description
Preliminary	Jun-4-2024	Advance Release.